CLAIMS

We Claim:

1. An apparatus, comprising;

an active semiconductor layer;

a transistor formed in the active silicon layer;

a bulk silicon layer having a first surface and a second surface;

an oxide layer formed between the active silicon layer and the first surface of the bulk silicon layer; and

a heat sink formed in the bulk silicon layer and configured to sink heat sourced through the oxide layer to the second surface of the bulk silicon layer.

2. The apparatus of claim 1, wherein the heat sink is a thermally conductive material provided in a plug formed in the bulk silicon layer.

3. The apparatus of claim 2, wherein the thermally conductive material is a metal.

4. The apparatus of claim 3, wherein the metal includes but not limited to one of the following types of metals: copper, aluminum, gold, tungsten.

5. The apparatus of claim 2, wherein the thermally conductive material is DAG (thermally conductive paste)

6. The apparatus of claim 1, wherein the transistor is an MOS transistor.

7. The apparatus of claim 1, wherein the transistor is a bipolar transistor.

8. The apparatus of claim 1, further comprising isolation regions formed around the transistor in the active silicon layer and contacting the oxide layer formed between the active silicon layer and the first surface of the bulk silicon layer.

9. The apparatus of claim 1, wherein the heat sink is substantially plug shaped.

10. The apparatus of claim 9, wherein the plug has a length substantially the same as the thickness of the bulk silicon layer.

11. The apparatus of claim 9, wherein the plug has a circumference ranging from 1 to 50000 microns.

12. The apparatus of claim 1, further comprising

a plurality of transistors formed in the active region, and

a plurality of heat sinks associated with the plurality of transistors respectively, each of the plurality of heat sinks formed in the bulk silicon layer configured to sink heat sourced in the oxide layer to the second surface of the bulk silicon layer.

13. The apparatus of claim 12, wherein the plurality of transistors and the plurality of heat sinks are formed on a semiconductor die.

14. The apparatus of claim 12, wherein the plurality of transistors and the plurality of heat sinks are formed on a semiconductor wafer.

15. The apparatus of claim 1, wherein the bulk silicon layer is formed in a semiconductor material having one of the following orientations: 100, 111, or 110.

16. The apparatus of claim 1, wherein the active silicon layer is formed in a semiconductor material having one of the following orientations: 100, 111, or 110.

17. A method comprising:

providing an oxide layer between an active region and a bulk region on a semiconductor wafer;

fabricating a transistor in the active region on the semiconductor wafer; and

forming a heat sink in the bulk region of the semiconductor wafer adjacent the transistor, the heat sink extending from the oxide layer through the thickness of the bulk region of the semiconductor wafer.

18. The method of claim 17, wherein the heat sink is formed by etching bulk region to form a plug in the bulk region, the plug extending from the oxide layer through the thickness of the semiconductor wafer.

19. The method of claim 18, further comprising filling the plugs with a thermally conductive material.

20. The method of claim 19, wherein the thermally conductive material includes one of the following types of thermally conductive materials: copper, aluminum, gold, tungsten, DAG (thermally conductive paste).

21. The method of claim 17, wherein the etching is an anisotropic plasma etch.

22. The method of claim 17, wherein the etching is a wet etch.

23. The method of claim 22, wherein the wet etch is ethanol wet etch.

24. The method of claim 17, wherein the transistor is a MOS transistor.

25. The method of claim 17, wherein the transistor is a bipolar transistor.